B.E. (Computer Technology) Third Semester (C.B.S.)

Computer Architecture & Organization Paper – V

P. Pages : 2 **TKN/KS/16/7324**

Time : Three Hours * 1 0 8 9 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) What is addressing Mode? Explain different Addressing modes with example. **10**

b) Draw and explain stored program architecture. **4**

OR

2. a) What are subroutines? Explain the execution sequence of nested subroutines. **5**

b) Explain how instruction sequence is done in CPU while executing a program. **5**

c) Write Assembly Language program to add five numbers stored in the memory. **4**

3. a) Explain Instruction formats used in IBM-370 system. **7**

b) Explain the limitations of short word length machines. **6**

OR

4. a) Write down the control sequence for fetching a word from memory using single bus organization. **7**

b) Write and explain the control sequence for execution of complete instruction. **6**

5. a) Explain the difference between hardwired control unit and microprogrammed control unit with neat diagram. Is it possible to have hardwired control associated with a control memory **7**

b) Write short notes on **6**
i) Bit slice ALU.
ii) Microinstructions with next address field.

OR

6.	a)	What is horizontal and vertical microinstruction format? Explain grouping of control signals with suitable example.	**9**
	b)	Explain Emulation.	**4**
7.	a)	Solve the following using Booth's algorithm. 13 x (– 6) Explain how Booth's algorithm different from bit pair recording method.	**8**
	b)	What are the exceptions in floating point arithmetic? Represent $\frac{1}{32}$ and $\frac{1}{16}$ in IEEE single and double precision format.	**5**

OR

8.	a)	What are guard bits? State their necessity. How they are removed?	**5**
	b)	Perform 17/3 integer division by using restoring and non-restoring division algorithm.	**8**
9.	a)	What is memory interleaving? Explain whether speed of execution is improved with its use.	**7**
	b)	Consider a cache consisting of 16 words. Each block consists of 4 words. Size of the main memory is 256 bytes. find the number of bits in each of TAG, BLOCK/SET and WORD for associative mapped cache?	**6**

OR

10.	a)	Explain how virtual address is translated into physical address in virtual memory technique.	**7**
	b)	Draw and Explain the operation of static DRAM memory cell.	**6**
11.	a)	Compare RISC with CISC.	**6**
	b)	Write a short note on Array processors.	**8**

OR

12.		Write short notes on **any three**.	
	i)	Vector processor.	**5**
	ii)	Multicore architecture.	**5**
	iii)	Flyn's classification of parallel structure.	**4**
	iv)	Loosely coupled and tightly coupled system.	**4**

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