PMM/KS/15/6931/6936

Faculty of Engineering & Technology

Third Semester B.E. (Electronics Engg./ET/EC)

(C.B.S.) Examination

ELECTRONIC DEVICES AND CIRCUITS

Time—Three Hours] [Maximum Marks—80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.

(2) Answer **SIX** questions.

(3) Due credit will be given to neatness and adequate dimensions.

(4) Assume suitable data wherever necessary.

(5) Illustrate your answers wherever necessary with the help of neat sketches.

(6) Use of non-programmable calculator is permitted.

SUMMER– 15

1. (a) Compare transition capacitance and diffusion capacitance. 3

(b) Explain effect of temperature on diode current. 3

(c) Two similar P-N junction Ge diodes are connected in series opposing A 6V battery is impressed upon the series arrangement. Find the voltage across each junction at room temperature. The breakdown voltage is greater than 6V. 7

OR

2 (a) Explain bridge rectifier with the help of diode current, output current and output voltage waveform. Explain peak inverse voltage for this circuit and derive expression for average current. 6

(b) Show that maximum rectification efficiency of full wave rectifier is 81.2%. 7

3. (a) Explain how BJT works as an amplifier. 5

(Contd.)

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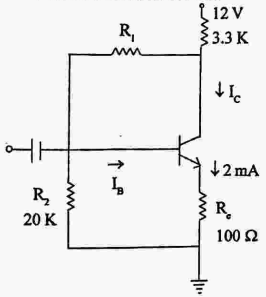
(b) If $\alpha = 0.98$ and $V_{BE} = 0.7V$, find R_1 in the circuit shown for an emitter current of 2 mA. Neglect the reverse saturation current. 6



(c) Compare different regions of BJT with respect to their dimension and doping level. 3

OR

4. (a) What is the necessity of biasing for BJT circuit ? 4

(b) Define Stability factors. 3

(c) Explain self bias circuit and derive its equation of stability. 7

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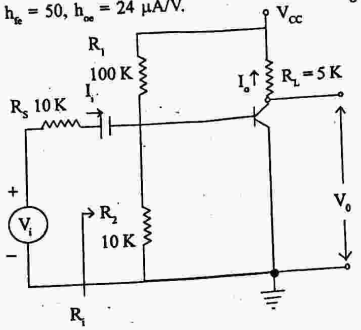
5. (a) Compare CE, CB and CC configurations. 5

(b) Calculate $A_I = \frac{I_o}{I_i}$, A_V, A_{VS}, R_o and R_i for given circuit. Assume h_{ie} = 1100 Ω, $h_{re} = 2.5 \times 10^{-4}$, h_{fe} = 50, h_{oe} = 24 μA/V. 8



OR

6. (a) Explain advantages of negative feedback amplifiers in detail. 6

(b) When negative feedback is applied to an amplifier having gain 100, the overall gain falls to 50.

(i) Calculate the fraction of output voltage feedback.

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(ii) If this feedback fraction is maintained, calculate the value of the amplifier gain required if the overall gain is to be 75. 7

7. (a) Explain crystal oscillator. Derive expression of resonant frequencies. 7

(b) A Hartley oscillator is designed with L_1 = 2 mH, L_2 = 20 μH and a variable capacitance. If the frequency of oscillation is varied between 0.9 MHz and 2.1 MHz, find the range of capacitance values. 6

OR

8. (a) Explain working of astable multivibrator with its circuit diagram. 6

(b) Explain Barkhausan's criteria of oscillation. 3

(c) Draw and explain working of RC phase shift oscillator. 4

9. (a) Explain Class B push pull power amplifier. Calculate its conversion efficiency. 6

(b) Calculate the harmonic distortion for an output signal of a power amplifier having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third of 0.15 V and fourth of 0.05 V. 7

OR

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10. (a) What is harmonic distortion in power amplifiers and how it can be reduced ? 6

(b) With a load of 4 Ω, a push pull amplifier takes 3.25 A from the d.c. supply, with the sinusoidal signal. If V_{CC} = 24 volts, find the conversion efficiency. 7

11. (a) Explain static drain characteristics of JFET. 5

(b) For JFET, if I_{DSS} = 20 mA, $V_{GS(off)}$ = –5V and g_{mo} = 4 ms, determine the transconductance for V_{GS} = – 4 V and find I_D at this point. 6

(c) How JFET works as voltage variable resistance ? 3

OR

12. (a) Compare BJT and FET. 4

(b) The amplifier stage shown uses n-channel FET with I_{DSS} = 1 mA and V_P = –1V. Find the resistance R_1 if the quiescent drain to ground voltage is 10 V. 6

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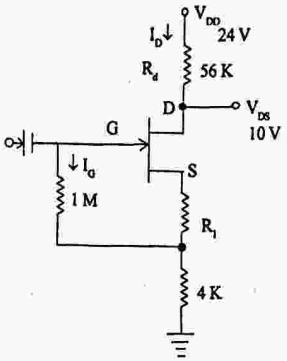

(c) Explain the enhancement effect in MOSFET. 4