Faculty of Engineering & Technology Third Semester B.E. (Electronic/ET/EC) (C.B.S.) Examination ELECTRONICS DEVICES AND CIRCUITS

Time—Three Hours]

[Maximum Marks-80

INSTRUCTIONS TO CANDIDATES

- (1) All questions carry marks as indicated.
- (2) Answer SIX questions
- (3) Due credit will be given to neatness and adequate dimensions.
- (4) Assume suitable data wherever necessary.
- (5) Illustrate your answers wherever necessary with the help of neat sketches.
- (6) Answer the questions as per choice given.
- (a) Write a short note on capacitive effect of P-N junction diode.
 - (b) Given Si diode with forward voltage of V=0.4V. Calculate the factor by which the current will be multiplied when the temperature is increased from 25°C to 150°C.

OR

2. (a) Draw the circuit diagram of full wave bridge rectifier

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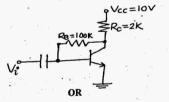
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and explain its operation. Also derive the expression for ripple factor and efficiency for full wave rectifier.

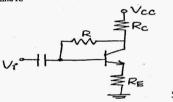
- (b) A full wave rectifier with capacitor filter is to supply a current of 20 mA at 16 V of f = 50 Hz and the allowed ripple of 1%. Calculate:
 - Secondary voltage of transformer
- (ii) The value of capacitor. 5
 3. (a) What are the different methods used for biasing of transistor? Explain any one method of biasing a
 - single stage BJT.

 (b) For the circuit shown below:
 - (i) Find I_B , I_C and V_{CE} , if Si-transistor with $\beta = 50$ is used
 - (ii) Specify R_B so that $V_{CE} = 7V$.



4. (a) Draw and explain the Ebers-Moll's model of a NPN transistor. 5

- (b) Discuss Early effect or Base Width modulation in transistor.
- (c) In the circuit shown V_{cc} = 24V, R_c = 10 k Ω , R_E = 270 Ω for Si transistor with β = 45 and V_{CE} = 5V, find R.



- 5. (a) Show block schematically the different feedback connections in an amplifier. Explain the effect of each type of feedback on input and output impedance.
 - (b) The overall gain of the two stage amplifier is 200 with negative feedback of 20% applied only to the second stage. Assuming that the first stage has negligible distortion and that the second stage has a gain of 300 and 10% distortion without feedback. Find (i) the distortion of second stage with feedback.
 (ii) The gain of the first stage.
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OR

- 6. (a) Explain the effect of negative feedback on :
 - (i) Voltage gain

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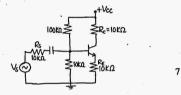
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- (ii) Bandwidth and
- (iii) Noise

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- (b) The transistor amplifier shown in figure below has a parameter given below:
 - hie = 1.1 k Ω , hre = 2.5×10⁻⁴, hre = 50, hoe =2.5 μ A/V. Calculate A₁, A₁, A₂, Zi and Zo.



- (a) Draw and explain the working of Wien Bridge oscillator. Also derive the expression for frequency of oscillation.
 - (b) State the conditions under which a feedback amplifier works as an oscillator.
 - (c) Determine the series and parallel resonant frequencies and quality factor for a Quartz crystal. Given that L = 150 μH, R = 7Ω, C = 0.025 pF and C_m = 0.4 pF.

OR

(a) Draw the circuit diagram for Colpitt's oscillator and explain its working.

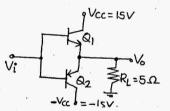
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- (b) Draw the circuit diagram of transistorized Astable multivibrator and explain its working with waveform.
- (a) Show that the efficiency of transformer coupled power amplifier in class A is 50%.
 - (b) Draw the schematic diagram of class-B push-pull amplifier and show that output consists of odd harmonics only.

OR

- 10. (a) What is Cross-over distortion in amplifier? How can it be eliminated?
 - (b) The ideal class-B push-pull amplifier shown with V_{cc} = 15V, R_{\downarrow} = 5 Ω and the input signal. Determine:
 - i) Maximum output signal power
 - (ii) Maximum d.c. input power
 - (iii) The conversion efficiency.
 - (iv) What is the maximum dissipation of each transistor and what is the efficiency under these conditions?



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- 11. (a) Draw and explain common source drain-characteristics of an n-channel JFET. 5
 - (b) Draw mutual characteristics of JFET and show that:

$$g_{m} = \frac{2}{|V_{p}|} \sqrt{I_{DSS} \cdot I_{DS}}$$

(c) Compare BJT and JFET.

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OR

- 12. (a) Explain the working of P-channel Depletion type MOSEFT with neat diagram and draw the characteristics also.
 - (b) A bias circuit FET is shown in figure below. Determine the quiescent values of V_{DS} , V_{GS} and ID. Given that $V_{p} = -5V$, $I_{DSS} = 5mA$ 7

