VRK/KS/14/6588

Faculty of Engineering & Technology
Third Semester B.E. (Computer Technology) (C.B.S.)
Examination
COMPUTER ARCHITECTURE AND ORGANIZATION
Paper—V

Time—Three Hours] [Maximum Marks—80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.

(2) Due credit will be given to neatness and adequate dimensions.

(3) Assume suitable data wherever necessary.

(4) Diagrams should be given wherever necessary.

(5) Illustrate your answers wherever necessary with the help of neat sketches.

1. (a) Write an Assembly Language Program using loop that multiplies two positive numbers by using repeated addition. For example, to multiply 3 and 6, the program would add 3 six times, or 3+3+3+3+3+3. 4

(b) Write an Assembly Language Program to add five numbers stored in the memory. 3

(c) Consider the following possibilities for saving the return address of a subroutine :

(i) In a processor register

(ii) In a memory location associated with the call, so that different location is used when subroutine is called from different places.

(iii) On a stack.

Which of these possibilities supports subroutine nesting and which supports subroutine recursion and why ? 7

OR

2. (a) Register R_5 is used in a program to point to the top of stack containing 32-bit numbers. Write a sequence of instruction using Index, Autoincrement and Autodecrement addressing modes to perform each of following tasks :

(i) Pop two items off the stack, add them and push result onto stack.

(ii) Copy fifth element from top into register R_3.

(iii) Remove top ten items from the stack.

For each case, assume stack contains ten or more elements. 6

(b) What do you mean by addressing mode ? Explain with example the necessity of different addressing modes ? 8

3. (a) Write control sequence for execution of following instruction

SUB (R_1) +, 1000

clearly mention each step by giving its function performed. Assume single bus processor architecture and each instruction consists of two words. 6

(b) Explain instruction formats used in IBM 370. 7

OR

4. (a) Explain 3 bus architecture with neat diagram. 6

(b) Write a program to evaluate the expression

$(A \times B + C \times D)/E * F$

(i) In a single accumulator processor, assume that processor has Load, Store, Multiply and add instruction and that all values fit in accumulator.

(ii) Write a program using stack.

(iii) Write a program assuming three address instruction. 2.5+2.5+2

5. (a) Give microinstruction for

Add $R_{src.}$ (R_{dst}) 6

(b) Explain the difference between hardwired control and microprogrammed control with neat diagram. Is it possible to have a hardwired control associated with a control memory ? 7

OR

6. (a) In a computer instruction format, the instruction length is 11 bits and size of an address field is 4 bits. Is it possible to have :

5, 2-address instructions

45, 1-address instructions

32, 0-address instructions

using this format ? Justify your answer. 7

(b) Explain horizontal and vertical organization used in microprogrammed control. 6

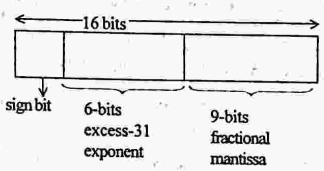
7. (a) What are guard bits ? How can guard bits be removed ? State their necessity. 5

(b) Describe the implementation of 4 bit carry look ahead adder. How can it be extended to higher number of bytes ? What is maximum gate delay generated by a 4 bit parallel binary adder and how can it be minimized by carry look ahead adder ? 8

OR

8. (a) Divide 38 by 7 using non-restoring division method. 5

(b) Consider the floating numbers are represented in 16-bit format, as shown in figure. Represent 12.5 and – 6.25 in this format. Also multiply these two numbers using floating point multiplication algorithm.



8

9. (a) Design 4 M × 32 memory using 512 k × 8 static memory chips. 6

(b) What is virtual memory ? With suitable diagram explain how logical address is converted to physical address. 7

OR

10. (a) With neat sketch, explain the utility of memory interleaving. 5

(b) Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume direct mapped Cache consists of 32 cache blocks :

(i) How is 16-bit main memory address divided ?

(ii) Into what block would bytes with each of the following addresses be stored ?

0001 0001 0001 1011

1100 0011 0011 0100.

(iii) How many total bytes of memory can be stored in Cache ?

(iv) Why tag is stored in Cache ? 3+2+1+2=8

11. (a) Give features of RISC processor. 5

(b) What is interrupt service routine ? Explain different mechanism available for handling interrupts. 9

OR

12. Write short notes on (any **THREE**) :

(a) Vector processor

(b) Array processor 3

(c) Multi core Architecture

(d) Flynn's classification of parallel structure. 14