SRK/KW/14–7008

Fourth Semester B. E. (Comp. Tech.) (Credit Base System) Examination

ADVANCED MICROPROCESSOR AND INTERFACING

Paper - III

Time : Three Hours] [Max. Marks : 80

N. B. : (1) All questions carry marks as indicated.
(2) Due credit will be given to neatness and adequate dimensions.
(3) Assume suitable data wherever necessary.
(4) Illustrate your answers wherever necessary with the help of neat sketches.

1. (a) Explain the operations carried out by BIU of 8086. 6

(b) Map 32 KB ROM and 32 KB RAM with 8086 µp, IC's available are 16 KB ROM and 8 KB RAM, using technique of mapping without fold back. 7

OR

2. (a) Explain the advantages of segmentation of memory in 8086 µp,. 6

(b) Write 8086 ALP to scan a constant ODH in a block using string instruction, the length of the block is at 2000: 2240 H, the block starts at 3000: 2240H, place 00 H at 2000: 2230 H if constant is found otherwise set memory location 2000 : 2230 H to all ones. 7

3. (a) Interface 8 ON OFF switches with 8086 µp using 74244 (Buffer). 4

(b) Interface four seven segment display with 8086 µp using 8255, segment driver, digit driver. Explain the technique of multiplexing. 10

OR

4. (a) Interface 8 LED's using 8255 with 8086 µp, write 8086 ALP to ON OFF LED with a delay. 7

(b) Write 8086 ALP to generate a square wave form of 1 KHz using timer 8253, when PCLK 2.5 MHz is available, show the interfacing with 8086 µp. 7

5. (a) Explain the initialisation of 8259 if port addresses are FOH and F2H for the following :—

(i) IRs accepted +ve edged trigerred.

(ii) Slave is connected to IR4 input of master.

(iii) n = 32 d, for master and n = 64 d for slave

(iv) Select SFNM for master. 7

(b) Using 8259 it is required to interrupt 8086 by 15 I/O devices, design a circuit, with suitable port addresses. 6

OR

6. (a) Explain the mode select command byte and control select command byte for 8251. 6

(b) Write 8086, ALP to send a message "FOURTH SEM" serially with 9600 Baud rate if frequency of 153.6 KHz is available with one stop bit, no parity error and 8 bit character using status check technique. 7

7. (a) State the difference between min. and maximum mode of 8086 µp. 6

(b) Draw and explain the architecture of 8087 NDP. 7

OR

8. (a) Interface 8 x 8 keyboard matrix and 8, seven segment displays with 8086 µp using 8279. 7

(b) Explain the BAR, CAR, BTR, CTR AR- Address register TR-Terminal count register, also explain the REQ, HLDA pins of 8237 PDMAC. 6

9. (a) Explain how the internal banks of 8051 are selected, state the bit accessible register, and GPR space of RAM, State the instructions to access the GPR. 6

(b) Write 8051 ALP to find the no. of negative data bytes in a block. The length of block is at 40 H, The block starts at 414, place the no. of negative data bytes at 30 H. 7

OR

10. Explain in detail internal architecture of 8051 µp 13

11. (a) Explain pipelining in a Pentium processor. 7

(b) Explain floating point unit of Pentium. 7

OR

12. (a) Draw and explain IDT descriptor of Pentium processor. 7

(b) What is protection provided in Pentium processor ? 7