

DSP Processor & Architecture

P. Pages : 2

Time : Three Hours



TKN/KS/16/7530/7538

Max. Marks : 80

- Notes :
1. All questions carry marks as indicated.
 2. Solve Question 1 OR Questions No. 2.
 3. Solve Question 3 OR Questions No. 4.
 4. Solve Question 5 OR Questions No. 6.
 5. Solve Question 7 OR Questions No. 8.
 6. Solve Question 9 OR Questions No. 10.
 7. Solve Question 11 OR Questions No. 12.
 8. Due credit will be given to neatness and adequate dimensions.
 9. Assume suitable data whenever necessary.
 10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Distinguish between single Access RAM and double Access RAM used in on-chip memory of TMS320CSX processor. Explain how memory access is increased in programmable DSPs ? 7
- b) Explain what is meant by instruction pipelining ? A non pipelined system takes 100ns to process a task. The same task can be performed in 4 segments pipelined into 20ns each. Determine speedup ratio of pipeline for 1000 tasks. 7
- OR**
2. a) Draw basic block diagram of MAC unit used in PDSPs. Explain how it is used to perform convolution. 6
- b) Describe the circular addressing mode with example. 4
- c) What is range of numbers that can be represented in a fixed point format using 16 bits, if the numbers are treated as. 4
- i) Signed integers ii) Signed fractions
3. a) What is status register ? List bits of STO of 5X and their functions. 4
- b) Explain direct addressing mode of C5X. Explain execution of instruction ADDC 20h with address generation process if content of DP=06 h and content of data memory location 0320h to 032f h are 20h. Take content of ACC as 30 h. 9
- OR**
4. a) Explain bus structure of TMS320C5X PDSP. 7
- b) Let the content of ARP, AR2 and INDX register be 2, 1250 h and 2 h respectively and contents of data memory location 1240 h-1260 h be filled with the data 2345 h. Let SXM be 0. Find the value of ACC and AR2 after sequential execution of following instructions. 6
- i) LACC *,0 ii) LACC *,1
- iii) LACC *,-3
5. a) Explain any three of the following instructions. 6
- i) MACD ii) ADD*,1
- iii) SUB#2345 h, 1 iv) BD PGM 1250 h

- b) Draw the table showing the content of the instruction pipeline when following program is executed. Explain. **7**
ZAP
BD PGM 1250 h
ADD *
SACL * +
MAC 4500 h, 25 h
PGM1250 h: LACC * +

OR

6. a) Draw block diagram of DSP starter kit C5XDSK. What are the addresses of the program memory address space and data memory address space in the DSP starter kit where user programs and data may be stored ? **8**

- b) Mention few applications of each of the families of TI DSPs. **5**

7. a) Explain data addressing modes of TMS320C54X processor. **8**

- b) Explain program control unit of TMS320C54X. **5**

OR

8. a) Explain how interrupts are handled in TMS320C54X P DS P ? **6**

- b) Draw and explain central processing unit of C54X in detail. **7**

9. a) List the features of TMS320C6X processor. **7**

- b) Give the brief introduction of Motorola DSP563XX processor. **7**

OR

10. a) Compare the features of C5X, C54X, and C6X in detail. **8**

- b) Write steps for creating new project and building Assembly language code in CCS. **6**

11. a) Explain filtering of long data sequence using overlap save method. **3**

- b) Find the output $y(n)$ of a filter whose impulse response is $h(n) = \{9, 10\}$ and input signal $x(n) = \{1, 2, 3, 4, 5, 6, 7, 8\}$ Using overlap add method. **10**

OR

12. a) Input sequence of 75 elements is to be convolved with an impulse response of a filter with 45 elements using FFT and IFFT. Determine total number of complex multiplications and additions needed to implement the convolution. The computation is to be implemented on a fixed point signal processor that takes 10 ns to do a real integer multiplication. Determine the computation time for complex multiplications involved. **8**

- b) Explain digital decimation filter implementation for decimation factor = 2 using 3-tap FIR filter. **5**
