B.E. (Electronics Engineering / Electronics & Telecommunication / Electronics & Communication Engineering) Seventh Semester (C.B.S.)

Advanced Digital System Design

P. Pages : 2 **TKN/KS/16/7533/7541**

Time : Three Hours * 1 0 2 8 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Questions 1 OR Questions No. 2.
3. Solve Questions 3 OR Questions No. 4.
4. Solve Questions 5 OR Questions No. 6.
5. Solve Questions 7 OR Questions No. 8.
6. Solve Questions 9 OR Questions No. 10.
7. Solve Questions 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Explain the different design units used in VHDL with their syntax. **7**

b) Explain brief history of VHDL. **4**

c) List typical advantages of HDLS. **3**

OR

2. a) Discuss Various levels of abstractions in VHDL. **7**

b) What is the difference between VHDL language and software language? **3**

c) Write VHDL code of 2 input XOR gate. **4**

3. a) How are scalar data types classified? Explain real and integer data type in brief. **6**

b) Explain in brief VHDL data objects with suitable example. **7**

OR

4. a) Write a VHDL code for a 3 to 8 decoder using a selected signal assignment statement. **7**

b) Write a VHDL code for a 4 to 2 priority encoder using conditional signal assignment statements. **6**

5. a) Write a VHDL code for a Four bit adder using structural modelling. **7**

b) What is subprogram? Explain 'Function' and 'Procedure' with their syntax. **7**

OR

6. a) Write a VHDL code for BYTE ADDER circuit using GENERATE statement. **8**

b) Write a test bench to test the functionality of 16 to 1 multiplexer. **6**

7. Write a difference between Moore and mealy circuits. Design a sequence detector for 0101 with mealy state machine and implement it with D flip-flop and write a VHDL code for the same. **13**

OR

8. A Fundamental mode circuit has inputs X_1 and X_0 and a single output Z. When $X_1X_0 = 00$, Z = 0. To make Z = 1, we start with $X_1X_0 = 00$ and first change X_0 to 1 and next change X_1 to 1. To return Z to Z=0, we must return $X_1X_0 = 00$, the order of return being of no consequence. **13**

a) Make a primitive flow Table.
b) Eliminate redundant state if any.
c) Make a state assignment that avoids critical races.
d) Draw the logic circuits.

9. a) Explain the concept of synthesis? Explain step by step process of synthesis. **7**

b) Explain efficient coding style used for HDL synthesis. **6**

OR

10. Write short note on **any two**. **13**

i) Partitioning for synthesis.

ii) Pipelining in VHDL.

iii) Optimizing arithmetic Expression.

11. a) A combinational circuit is defined by the function. **7**

$F_1(A, B, C) = \Sigma(3,5,6,7)$

$F_2(A, B, C) = \Sigma(0,2,4,7)$

Implement the circuit with a PLA having three inputs, four product terms and two outputs.

b) Explain the architecture of FPGA with neat diagram. **6**

OR

12. a) Design 4-bit left shift barrel shifter and write VHDL code for it. **6**

b) Write VHDL code for 3x3 binary multiplier using structural modelling. **7**

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