B.E. (Electronics / Electronics & Telecommunication /
Electronics Communication Engineering) Semester Seventh (C.B.S.) -

DSP Processor & Architecture (DSPA)

P. Pages : 2 **KNT/KW/16/7443/7451**

Time : Three Hours * 0 8 2 1 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Illustrate your answers whenever necessary with the help of neat sketches.
9. Use of non programmable calculator is permitted.
10. Due credit will be given to neatness and adequate dimensions.

1. a) Explain the difference between von-Neumann and modified Harvard Architecture. **7**

b) Explain what is meant by Instruction pipelining? A non-pipelined system takes 80ns to process a task. The same task can be performed in 4 segments. pipelined into 20ns each. Determine speedup ratio of pipeline for 1000 tasks. **7**

OR

2. a) Draw basic block diagram of MAC unit used in PDSPs? Explain how it is used to perform convolution. **7**

b) Distinguish between multiple access memory and multi ported memory. **7**

3. a) Explain the Architecture of DSP TMS320C5X. **6**

b) Explain the status register STO of TMS320C5X in detail. **7**

OR

4. a) Explain the addressing modes of TMS320C5X. **6**

b) Explain the statue register ST1 of TMS320C5X in detail. **7**

5. a) Write an assembly language program using instructions of TMS320C5X processors to multiply two numbers of unsigned 32 bit data. Assume that the two data are available in memory save the 64 bit product in memory. **10**

b) Describe the circular addressing mode with example. **3**

OR

6. a) Draw block diagram of DSP starter kit C5X DSK. What are the addresses of the program memory address space and data memory address space in the DSP starter kit where user programs and data may be stored? **10**

b) Explain the Instructions. **3**

i) MACD ii) LACC * +, 0

iii) SACH

7. a) Explain the Architecture of TMS320C54X in detail. **7**

b) Explain the following instructions **6**

i) LST ii) SAMM

ii) SAR iv) SACC

v) LACC vi) LDP

OR

8. a) Explain data addressing modes of TMS320C54X processor. **6**

b) Explain how interrupts are handled in TMS320C54X PDSP. **7**

9. a) Compare the features of C5X, C54X and C6X in detail. **7**

b) Explain the Architecture of Motorola DSP 563XX. **6**

OR

10. a) Write steps for creating new project and building Assembly language code in CCS. **6**

b) Draw and explain the architecture of TMS320C6X. **7**

11. a) Input sequence of 75 elements is to be convolved with an impulse response of a filter with 45 elements using FFT and IFFT. Determine total number of complex multiplications and additions needed to implement the convolution. The computation is to be implemented on affixed point signal processor that takes lons to do a real integer multiplication. Determine the computation time for complex multiplications involved. **8**

b) Explain wavelet transform and compare with Fourier transform. **6**

OR

12. a) Perform linear convolution of the following sequences by **8**
(a) overlap Add method and
(b) overlap save method.

x(n) = {1, -1, 2, -2, 3, -3, 4, -4};

h(n) = {-1, 1}

b) Explain the time complexity of DFT and FFT algorithm. **6**

****