B.E. Fourth Semester (Electrical Engineering (Electronics & Power)) (C.B.S.)
Digital & Linear Electronic Circuits (DLEC)

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Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.
11. Use of non programmable calculator is permitted.

1. a) Explain in detail the working of a two i/p TTL Nand gate with totem pole output. **7**

   b) Minimise the following function & implement it using two i/p NAND gates. Use k-map **7**
   $F(A, B, C, D) = \Sigma m(0, 13, 14, 15) + \Sigma d(1, 2, 3, 9, 10, 11)$

OR

2. a) Implement the following Boolean function using 8:1 MUX **7**
   $F(A, B, C, D) = \Sigma m(2, 4, 6, 7, 9, 10, 11, 12, 15)$

   b) Design 1:16 Demux using 1:2 De-mux. **7**

3. a) Explain working of Positive level triggered S-R flip flop using NAND gate. **7**

   b) Write short notes on ROM, EPROM & EEPROM. **6**

OR

4. a) Convert : **6**
   i) S-R flip flop to J-K flipflop.

   ii) S-R flipflop into D type flipflop.

   b) Explain the working of master slave J-K flipflop & Explain how race around condition **7**
   can be eliminated.

5. a) Draw the circuit diagram of 4-bit ripple counter (asynchronous counter) using 'T' flipflop. **7**
   Explain the working of the same with suitable timing diagram.

   b) Design full adder using two half adders. **6**

OR

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6.	a)	Explain in detail Arithmetic logical unit with neat diagram.	7
	b)	Differentiate synchronous & Asynchronous counters.	6
7.	a)	Draw the block diagram of OP.Amp & Explain the function of each block.	6
	b)	What is differentiator? What are its limitations? How they are overcome in practical differentiator?	7

OR

8.	a)	Derive an expression for Gain of inverting & non inverting OP-Amp.	6
	b)	Design the circuit to implement the equation $V_0 = 3V_1 - 2V_2 + 2V_3 + 2V_4$. Assume $R_F = 100 k\Omega$.	7
9.	a)	Explain the circuit of positive clipper & negative clipper.	7
	b)	Draw & explain the circuit diagram of precision full wave rectifier.	7

OR

10.	a)	Design a second order low pass fitter at cut-off frequency of 1.2 kHz (Assume $C_1 = C_2 = 0.1 \mu f$)	7
	b)	Explain Schmitt trigger using OP-Amp.	7
11.	a)	Draw the internal block diagram of IC555 & explain its working.	7
	b)	Write short notes on 78xx & 79xx.	6

OR

12.	a)	Design a square wave generator using IC555 having output frequency of 10kHz & duty cycle of 60%. Assume $C = 0.01 \mu f$.	7
	b)	Write short notes on IC723 Voltage Regulator.	6

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