B.E.Third Semester (Electrical Engineering) (C.B.S.)

Electronics Devices & Circuits

P. Pages : 3 **NKT/KS/17/7226**

Time : Three Hours * 0 2 7 5 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.
11. Use of non programmable calculator is permitted.

1. a) Draw circuit diagram and explain characteristics of half-wave rectifier. Also derive the following for half wave rectifier. **8**
   1) Peak current Im
   2) Average value of current Idc
   3) Efficiency η
   4) Ripple factor

   b) Explain difference between zener and Avalanche break down. **5**

OR

2. a) Draw VI characteristics of PN- junction diode and explain how it depends upon temperature. **5**

   b) Write short notes on half wave voltage doubler. **3**

   c) The avalanche diode regulates at 50V over a diode current from 5 to 40 mA. The supply voltage v = 200v, Calculate R to allow voltage to regulates load current $I_L = 0$ up to $I_{L\,max}$. What is $I_{L\,max}$? **5**

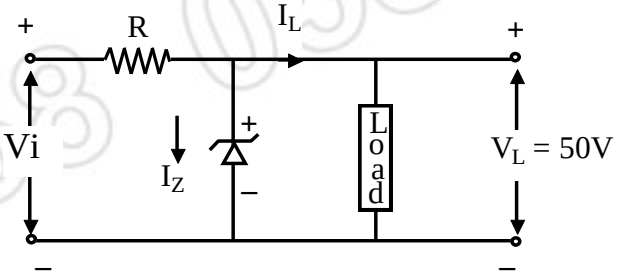


Figure of Q. 2 (c)

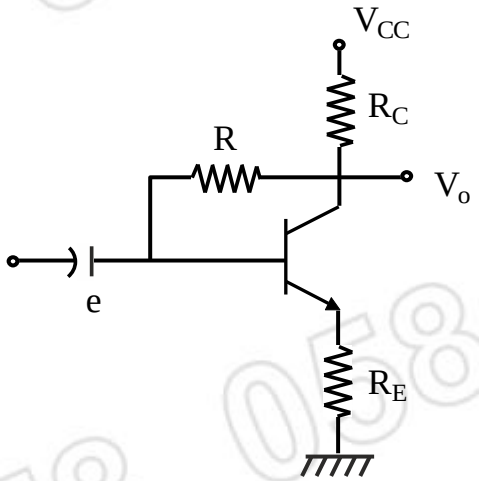
3. a) Compare CB, CE and CC transistor configurations and explain why CE configuration is most useful. **6**

b) Explain in brief thermal run away in a power transistor. What is bias compensation? Explain thermistor compensation. **8**

OR

4. a) Write the Eber's and Moll equations for BJT and sketch the circuit model which satisfies these equations. **5**

b) In the circuit shown in figure below $V_{CC} = 24\,v$, $R_C = 10k$ and $RE = 270\Omega$. If a silicon transistor is used with $\beta = 45$ and if $V_{CE} = 5V$, find R. Neglect the reverse saturation current. **5**



Figure

c) What is early effect and punch through effect in transistor. **4**

5. a) Draw the schematic diagram of class-B push pull amplifier and show that the maximum efficiency is 78.5% **8**

b) What is crossover distortion and How it is eliminated? **5**

OR

6. a) Explain the effect of negative feedback on bandwidth and gain of the amplifier. **6**

b) An amplifier without feedback gives a fundamental output of 36V, with 7% second harmonic distortion with input is 0.028V. **7**

i) If 1.2% of the output is feedback to the input in a voltage series feedback circuit, what is the output voltage.

ii) If the fundamental output is maintained at 36V but the second harmonic distortion is reduced to 1% what is input voltage?

7. a) Draw the circuit of crystal oscillator and explain its working. **5**

b) Draw and explain wein bridge oscillator circuit. Derive the expression for frequency of oscillation. **8**

OR

8. a) With the help of neat diagram explain the working of JFET. Also draw and explain static drain characteristics. **7**

b) Show that the transconductance g_m of a JFET is related to the drain current Ids by **6**

$$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \cdot I_{DS}}$$

9. a) What is the need of level shifting stage? Also, write the various level shifting techniques available. **6**

b) Explain in brief constant current bias circuit and current mirror circuit. **8**

OR

10. Draw the circuit of Dual input balanced output differential amplifier and Derive the equations for operating point V_{CEQ}, I_{CQ}, differential gain Ad, input resistance Ri, output resistance R_0 and CMRR. **14**

11. a) State and prove DeMorgan's Laws. **5**

b) Prove that **8**

i) $A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C = B + C$

ii) $(A + B + CD)\ (\overline{A} + B)\ (\overline{A} + B + E) = \overline{A}CD + B$

OR

12. a) Convert the following. **8**

i) $(543 \cdot 265)_{10} = (?)_8$

ii) $(1024)_{10} = (?)_{16}$

iii) $(101101 \cdot 10101)_2 = (\ )_{10}$

iv) $(26AF \cdot 78C) = (?)_2$

b) Simplify using Boolean laws and realize it by using NAND gate only: **5**

$\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$

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