B.E.Eighth Semester (Electronics & Telecommunication / Electronics & Communication Engineering) (C.B.S.)

Elective - III : CMOS VLSI Design

P. Pages : 2 **NKT/KS/17/7570**

Time : Three Hours * 0 3 3 4 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.
10. Use of non programmable calculator is permitted.

1. a) Explain the operation of PMOS enhancement transistor. **7**

b) Derive the basic DC equations of MOS transistor in three regions of operation. **6**

OR

2. a) Calculate the native threshold voltage for a n transistor at 300°K for a process with a Si substrate with $NA = 18\times10^{16}/cm^3$, a SiO_2 gate oxide thickness 200 A°. (Assume $\phi_{ms} = -0.9\,V,\ Q_{fc} = 0$) **7**

b) Explain small signal model for a MOS transistor and find the expression for g_m and g_{ds} in linear and saturation region. **6**

3. Explain the five regions of operation of CMOS inverter DC transfer characteristics. Hence derive the expressions for the same. **14**

OR

4. a) Consider a CMOS inverter circuit with the following parameters. **8**
$V_{DD} = 3.3\,V,\ V_{to,n} = 0.6\,V,\ V_{to,p} = -0.7\,V,\ k_n = 200\,\mu A/v^2$ and $k_p = 80\,\mu A/v^2$.
Calculate the noise margins of the circuit. The CMOS inverter being considered here has KR = 2.5 and $V_{to,n} \neq |V_{to,p}|$.

b) Design 4:1 multiplexer using transmission gates. **6**

5. Implement the following functions using CMOS logic gates - **13**

i) $Z = \overline{(A\cdot B)+(C\cdot D)}$ ii) $Z = \overline{A\,B\,C\,D}$

iii) $Z = \overline{A\,B\,C + D}$ iv) $Z = \overline{A}B + A\overline{B}$

OR

6. a) Explain the operation of a CMOS positive edge triggered D Flip Flop with a neat diagram. **7**

b) Design Ex-OR gate using CMOS logic gates. **6**

7. a) Derive the expression for static, dynamic and short circuit power dissipation and hence total power dissipation. **9**

b) Explain capacitance estimation of MOS device indicating accumulation, depletion and inversion region. **5**

OR

8. a) Explain switching characteristics of CMOS inverter and hence derive expression for rise time, fall time and delay time of a CMOS inverter. **9**

b) Write a short note on charge sharing. **5**

9. a) Explain Latch up in CMOS. How it is avoided. **6**

b) Draw stick diagram of - **7**
i) CMOS inverter -
ii) Two input NOR gate.

OR

10. Write short notes on **any three.** **13**

i) Domino Logic

ii) Clocking strategies.

iii) Transistor sizing.

iv) Fan in and Fan out.

11. a) State and explain different types of faults. **7**

b) What is DFT ? Explain in detail. **6**

OR

12. Write short notes on **any two.** **13**

a) BIST

b) Boundary scan technique.

c) JTAG

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