B.E. Seventh Semester (Electronics / Electronics & Telecommunication / Electronics & Communication Engineering) (C.B.S.)

DSP Processor & Architecture

P. Pages : 2 **NKT/KS/17/7443/7451**

Time : Three Hours * 0 0 8 5 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Illustrate your answers whenever necessary with the help of neat sketches.
10. Use of non programmable calculator is permitted.

1. a) Draw basic block diagram of MAC unit and explain how convolution is performed using a single MAC unit. **7**

b) A non pipelined system takes 100 nsec to process a task. The same task can be performed in 5 segments pipelined into 10 nsec each. Determine speed up ratio of pipeline for 1000 tasks. **6**

OR

2. a) Explain the difference between Von Neumann and Harvard architecture for the processor. Which architecture is preferred for DSP applications and why? What is modified Harvard Architecture? **7**

b) A DSP has a circular buffer with the start and the end addresses as 0210 h and 0201 h respectively. What would be the new value of the address pointer of the buffer if in the course of address computations, it gets updated to **6**

a) 0212 h b) 01FC h.

3. a) Draw the internal architecture diagram of 5X and indicate the various blocks. **8**

b) Let the content of ARP. AR_2 be 2, 1250 h respectively and contents data memory location 1240 h – 1260 h be filled with the data 2345 h. Let 5XM be 0. Find the value of ACC, AR2, ARP after execution of ADD *, 2 instructions. **6**

OR

4. a) What is status register? List bits of ST0 and ST1 of 5X and their functions. **8**

b) Let the content of ARP. AR2 and INDX register be 2, 1250 h and 2 h respectively and contents of data memory location 1240 h – 1260 h be filled with the data 2345 h. Let 5XM be 0. Find the value of ACC and AR2 after execution of following instructions. **6**

1) LACC *, 0 2) LACC * 0+, 1 3) LACC * – , 2

5. a) Explain following instructions. **8**

1) SUB 55 h, 2 2) LST #1
3) MACD 4) MPY

b) Draw the table showing the content of the instruction pipeline when following program is exerted. **5**

ZAP
BD PGM 1250 h
ADD
SACL+
MAC 4500 h, 25 h
PGM 1250 h : LACC+

OR

6. a) Draw block diagram of DSP starter kit C5X DSK. What are the addresses of the program memory address space and data memory address space in the DSP starter kit where user programs and data may be stored? **7**

b) Mention few applications of each of the facilities of TI DSPs. **6**

7. a) Explain internal memory organization of C54X. **6**

b) How many buses are there in C54X. Explain each in detail. **7**

OR

8. a) Explain phases of pipelining of TMS320C54X processor. **7**

b) Explain following data addressing modes of TMS320C54X processor. **6**
1) Absolute 2) Accumulator 3) Stack

9. a) List the features of TMS320C6X processor. **7**

b) Write a short note on Code Composer Studio (CCS). **6**

OR

10. a) Compare the features of C5X, C5AX and C6X in detail. **7**

b) Give the brief introduction of Motorola DSP563XX processor. **6**

11. a) Write short note on interpolation filter. **6**

b) Find the output y(n) of a filter whose impulse response is h(n)={9, 10} and input signal x(n)={1, 2, 3, 4, 5, 6, 7, 8} using overlap save method. **8**

OR

12. a) Input sequence of +5 elements is to be convolved with an impulse response of a filter with 45 elements using FFT and IFFT. Determine total number of complex multiplications and additions needed to implement the convolution. The computation is to be implemented on a fixed point signal processor that takes 10 ns to do a real integer multiplication. Determine the computation time for complex multiplication involved. **8**

b) Explain wavelet filter. **6**

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