B.E. Seventh Semester (Electronics / Electronics & Telecommunication / Electronics Communication Engineering) (C.B.S.) -

Advanced Digital System Design

P. Pages : 2 **NKT/KS/17/7446/7454**

Time : Three Hours * 0 0 8 6 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Diagrams and chemical equations should be given whenever necessary.
11. Illustrate your answers whenever necessary with the help of neat sketches.
12. Use of non programmable calculator is permitted.

1. a) Explain concurrency in VHDL with suitable example. **3**

b) Explain VHDL development. flow with suitable flow chart. **6**

c) Explain different approaches in VHDL. **5**

OR

2. a) What are the primary and secondary design units? Explain each with suitable syntax. **9**

b) Discuss various levels of abstraction in VHDL. **5**

3. a) Explain different data objects in VHDL. **8**

b) Design & write VHDL code for 1-bit full adder using Data-Flow. **6**

OR

4. a) Explain various data types in VHDL. **8**

b) Differentiate between conditional and selected signal assignment statements. **6**

5. a) Write a VHDL code for BCD to seven segment decoder. **7**

b) Write a VHDL code for 16:1 multiplexer using generate statement. **6**

OR

6. a) What do you mean by Port mapping? What are the types? Explain each with syntax. **6**

b) Write a VHDL code for Byte adder using generate statement. **7**

7. What is the difference between mealy and Moore state machine? Write a VHDL code for 1010 sequence using Moore state machine. (Use overlapping) **13**

OR

8. a) Draw the state diagram for **7**

i) D flip flop

ii) J-K flip flop

iii) T flip flop

b) Explain Races and critical races in digital circuits. **6**

9. a) What is pipe lining? Explain with an example. **5**

b) Explain power analysis of FPGA based system. **8**

OR

10. a) Explain timing analysis of logic circuits. **4**

b) Explain the term (Any two) **9**

i) Resource sharing

ii) Partitioning for synthesis

iii) Optimization of arithmetic expressions.

11. a) Explain place and route process in FPGA based system. **6**

b) Explain with suitable block diagram Xilinx 4000 series FPGA. **7**

OR

12. a) Write a VHDL code for 3-bit multiplier. **7**

b) Write VHDL code for 4-bit barrel shifter. **6**

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