B.E. Fifth Semester (Electronics / Electronics Telecommunication / Electronics Communication Engineering) (C.B.S.)

Analog Circuits & Design

P. Pages : 3 **NKT/KS/17/7325/7330**

Time : Three Hours * 0 0 0 8 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data whenever necessary.
4. Illustrate your answers whenever necessary with the help of neat sketches.
5. Use of non programmable calculator is permitted.

1. a) Draw the circuit diagram of emitter coupled dual input balanced output differential amplifier & derive its voltage gain in terms of collector resistor RC & AC emitter resistance re. **7**

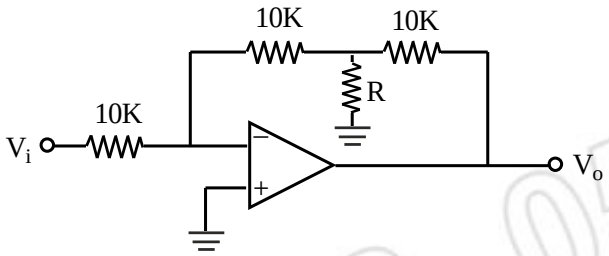
b) Define the following terms. **6**

i) Input offset voltage.
ii) Gain offset voltage.
iii) CMRR.
iv) Slew rate.

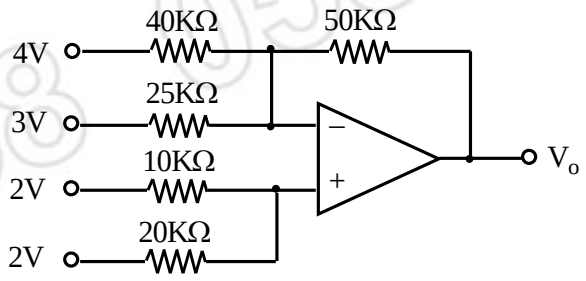
OR

2. a) Draw the basic building block of OP-Amp & explain the function of each block. **6**

b) For the circuit shown in figure below find the value of R required to obtain $V_o = -50V_i$. **7**



3. a) For the circuit shown, determine output voltage. Derive the necessary expression used **5**



b) Give the circuit diagram of an instrumentation amplifier using three op-amps and derive the expression for its output. **8**

OR

4. a) Draw the circuit of practical temperature compensated logarithmic amplifier and derive an expression for output voltage. **7**

b) Design integrator circuit to implement following equations : **6**

$$V_0 = -\frac{1}{3}\int V_1\,dt - \frac{1}{2}\int V_2\,dt - \int V_3\,dt$$

where V_1, V_2 and V_3 are input voltages and V_0 is output.

5. a) Draw the circuit diagram & explain the working of precision full wave rectifier. Derive the expression for output voltage. **7**

b) For a schmitt trigger circuit using op-amp shown in fig. 5(b) find out the volue of V_{LT} and V_{UT}. **7**
Assume $R_1 = 82k\Omega,\ R_2 = 2k\Omega$.

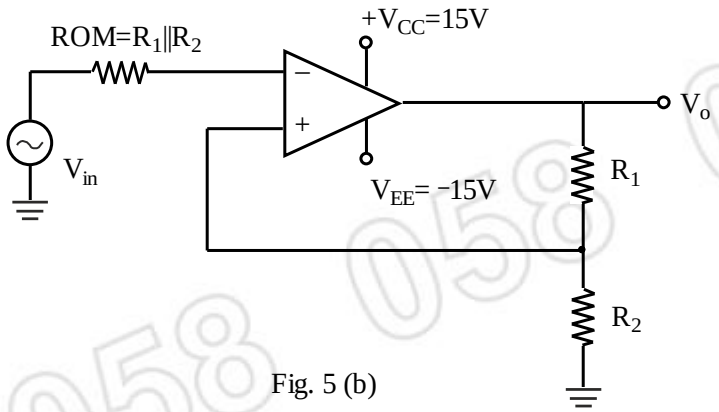


Fig. 5 (b)

OR

6. a) Write short notes on **any one.** **7**
i) Successive approximation type A to D converter.
ii) Sample and Hold circuit.

b) Explain with the help of Block diagram timer IC. 555. **7**

7. Design a series voltage regulator to give 5V output at a minimum load current of 500mA, use the following data for design $V_{in} = 15V \pm 10\%$ with source resistance of 5Ω for series pass element transistor θ_1 with $h_{fe_1} = h_{FE_1} = 40$ and error amplifier transistor θ_2 with $h_{fe_2} = h_{FE_2} = 100$, Calculate performance parameters. **13**

OR

8. a) Design a SMPs to give 12V at 5A, the unregulated input is 25V, the switching frequency is 25 kHz. The transistor used for switching has switching time of 1μ sec and saturation voltage $V_{sat} = 1V$. The fast recovery diode has $V_{DON} = 1V$. Assume reference of 1.8V. It is desired to have peak to peak ripple voltage of 30mV. Determine the efficiency of SMPS. Assume $I_{COFF} = 20\,mA$. **10**

b) Give comparison between SMPS and Linear regulators. **3**

9. a) Derive an expressions for frequency of oscillation in case of wein bridge oscillator. **6**

b) Design RC phase shift oscillator for the following specifications **8**
$V_0 = 8V$ peak to peak,
frequency of oscillations = 10 kHz.
Also determine frequency shift if
phase shift of 1° is introduced in the loop.

OR

10. Design a function generator to realise the equation $V_0 = V_i^2$. The range of input is 0 to 3. Assume at least three break points.

11. a) List out the advantages of active filters over passive filters. **4**

b) Design Butterworth filter such that relative attenuation is less than 1dB for frequencies below 500Hz and than 17dB for frequencies above 1 kHz. **10**

OR

12. a) Design a narrow band pass filter using 1GMF technique with pass band gain of 4, centre frequency of 100Hz and bandwidth of 0.1kHz. Derive the relation used. **10**

b) Write short notes on Relay driver circuit. **4**

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