B.E.Fourth Semester (Electronics / Electronics Telecommunication /
Electronics Communication Engineering) (C.B.S.)
Digital Circuits & Fundamentals of Microprocessors

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Notes : 1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.
11. Use of non programmable calculator is permitted.

1. a) Minimize the function and implement using NAND logic

$f(A, B, C, D) = A\overline{B}CD + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}\,B\,\overline{C}\,\overline{D} + ABCD$ **6**

b) Use K-MAP to solve the following. Also implement the result using universal gate logic only.   **8**
i) $f(A, B, C, D) = \sum m\,(0, 1, 4, 6, 7, 11, 12, 13, 15) + d(3, 10)$
ii) $F(P, Q, R, S) = \prod M(1, 4, 8, 10, 12, 13, 15) \cdot D(2, 11)$

OR

2. a) Design a code converter which will convert 3 bit binary number applied at the input into equivalent gray code.   **7**

b) Design and implement full adder from two half adders and one OR gate. Draw the logic circuit and give its truth table.   **7**

3. a) Design a BCD to seven segment decoder for common cathode configuration.   **8**

b) Design 1:32 demultiplexer using 1:8 demultiplexers & 1:4 DEMUX.   **5**

OR

4. a) Implement the following function using 8:1 multiplexer   **6**
$F(A, B, C, D) = \sum (0, 2, 4, 5, 7, 9, 12, 15)$

b) Design a decimal to BCD encoder and explain.   **7**

5. a) What is master slave J-K flip flop ? Explain with neat diagram. Also show it NAND logic implementation.   **9**

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	b)	Explain the use of preset and clear terminals in Flip-Flop.	**4**

OR

6.   a)   Convert the following Flip-Flop.   **8**
                          i)   S-R to J-K flip-flop.
                          ii)   J-K to T flip-flop.

        b)   Explain how latch can be used as a 1-bit memory cell.   **5**

7.   a)   Design and draw a 3-bit synchronous counter which passes through the following states.   **7**
                        $1 \rightarrow 3 \rightarrow 4 \rightarrow 6 \rightarrow 1$

        b)   Draw and explain 4-bit Ripple counter with waveforms.   **6**

OR

8.   a)   Draw the logic diagram of 4 bit bidirectional shift register and explain its working.   **8**

        b)   Explain twisted Ring counter with neat block diagram.

9.   a)   Define the following terms with respect to logic families.   **8**
                          i)   Speed of operation   ii)   Noise margin
                          iii)   Power dissipation   iv)   Fan in

        b)   Compare TTL and CMOS logic families with at least five points.   **5**

OR

10.   Write short notes on **any three.**   **13**

          i)   PAL device.

          ii)   SRAM memory.

          iii)   Types of Integrations.

          iv)   EPROM memory.

11.   a)   Draw and explain the architecture of 8085 microprocessor.   **9**

        b)   Explain the flag register of 8085 microprocessor.   **5**

OR

12.   a)   Explain various addressing modes of 8085 microprocessor. Also give one example for   **7**
                 each one.

        b)   Explain the following instructions of 8085 microprocessor.   **7**
                      i)   MOVA, M   ii)   DAA
                      iii)   CALL 1000H   iv)   XCHG

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