B.E. Third Semester (Computer Technology) (C.B.S.)

Computer Architecture & Organization

P. Pages : 3 **NKT/KS/17/7236**

Time : Three Hours * 0 2 8 3 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.

1. a) What are big endian and little endian technique? Give example of each. **6**

b) Write a program that can evaluate the expression A x B + C x D in a single accumulator processor. Assume that the processor has load, store, multiply and add instructions and that all values fit in the accumulator. **4**

c) Explain how instruction sequencing is done in a CPU while executing a program. **4**

OR

2. a) Convert the following pairs of decimal numbers to 5 - bit, signed, 2's complement, binary numbers and add them. State whether or not overflow occurs in each case. **8**

i) 5 and 10
ii) 7 and 13
iii) -14 and 11
iv) -5 and 7
v) -3 and -8
vi) -10 and -13

b) What are subroutine? Explain the execution sequence of nested subroutine. **6**

3. a) Write down the control sequence for fetching a word from memory using single bus organization. **7**

b) Explain 3 - address, 2 - address, 1 - address, and zero address instruction formats. **6**

OR

4. a) Draw and explain instruction formal of IBM 360/370 system. **6**

b) Write and explain the control sequence for an unconditional Branch instruction. **7**

5. a) Write the sequence of control steps required for the single bus structure for each of the following instruction. **6**

i) Add the (immediate) number NUM to register R_1.
ii) Add the content of memory location NUM to register R_1.
iii) Add the content of the memory location whose address is of memory location NUM to register R_1.

www.solveout.in

b) Differentiate between the hardwired and microprogrammed control. **5**

c) Explain bit - 0 Ring technique. **2**

OR

6. a) A system support 1 - address and 2 - address instruction. If the instruction length is 16 bits and the memory is having 64 words, how many 1 - address instruction exists if there are '4' 2 - address instruction? **5**

b) Define the following terms : **8**

i) control word

ii) control store

iii) micro routine

iv) microinstruction

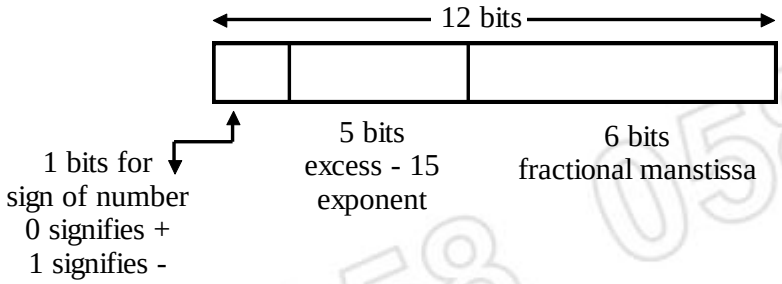
v) Bit Slice

7. a) Multiply the following pairs of signed 2's complement numbers using the Booth's and Bit - pairing of the multipliers algorithm, assume that A is the multiplicand and B is the multiplier A = 010111 and B = 110110. **8**

b) Perform $17 \div 3$ integer division by using restoring method. **5**

OR

8. a) Consider the floating numbers are represented in 12 bit format, as shown fig. Represent + 1.7 and - 0.012 in this format. **7**



b) Explain the design of fast address? **6**

9. a) Design $4M \times 32$ memory using $512K \times 8$ static memory chip. **6**

b) A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contain 512 bytes of data. **7**

i) What is the maximum number of bytes that can be stored in this unit?

ii) What is the data transfer rate in bytes per second of a rotation of speed 7200 rpm?

iii) Using a 32 - bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes per sector.

OR

www.solveout.in

10. a) A block set - associative cache consist of a total 64 blocks divided into 4 blocks sets. The main memory contains 4096 blocks, each consisting of 128 words. **5**

i) How many bits are there in a main memory address?

ii) How many bits are there in each of the TAG, SFT and WORD field.

b) What is meaning interleaving? Explain whether speed of execution is improved with its use. **6**

c) Explain page table. **2**

11. a) Give features of RISC & CISC processor. **7**

b) Write and explain the different technique of synchronous data transfers. **7**

OR

12. Write short notes on **any four.**

i) Pipelining. **3**

ii) Data Hazards **3**

iii) Peripheral devices **4**

iv) Array processor **4**

v) Vector processor **3**

****

www.solveout.in

www.solveout.in