B.E. (Electronics & Telecommunication /
Electronics & Communication Engineering) Semester Seventh (C.B.S.)
Elective - I : VLSI Signal Processing

P. Pages : 2

Time : Three Hours

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0835

Max. Marks : 80

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Notes : 1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Use of non programmable calculator is permitted.

1. a) Explain the structure of Direct form FIR filter and broadcast form of FIR filter. Show that the Data broadcast form can achieve a faster clock rate. **7**

   b) Design a parallel system for **6**
   $$y(n) = ax(n) + bx(n-1) + cx(n-2)$$
   With L (level of parallel processing) = 3
       n (Iteration factor) = 3 k
   Where K = no. of clock cycle.

   OR

2. a) How parallel processing can be used to reduce power consumption? Explain in detail. **6**

   b) What is fine grain pipelining? How can we use pipelining to reduce power consumption? **7**

3. a) Explain properties of Retiming with example. **7**

   b) Explain the method of Cutset Retiming and pipelining with slow down technique. **7**

   OR

4. Consider the data flow graph, construct the matrix W(U,V) and D(U,V) by manual Inspection. construct the set of unequalities for clock cycle of 2 solve the unequalities by creating a constraint graph and using Bellman - ford algorithm find Retimed graph. **14**
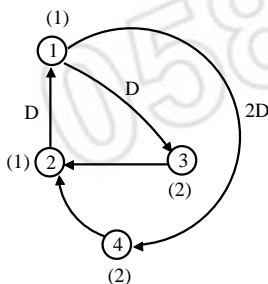
5. a) Give the properties of unfolding. Elaborate them with example. **7**

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b) Perform unfolding with unfolding factor J = 3 for the given fig. **6**
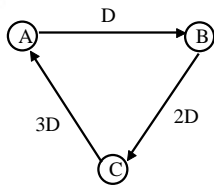
<div align="center">OR</div>

6. Describe how to design parallel processing architectures using unfolding. **13**

7. a) Explain the folding algorithm. **5**

b) Consider a DSP program that perform the transpose operation of 3x3 matrix. Find minimum number of registers required to implement the DSP program and give its folded architecture. **8**

The matrix = $\begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix}$

<div align="center">OR</div>

8. a) Explain life - time analysis for register minimization. **5**

b) Design folded biquad filter by systematic folding technique for the fig. given below: **8**
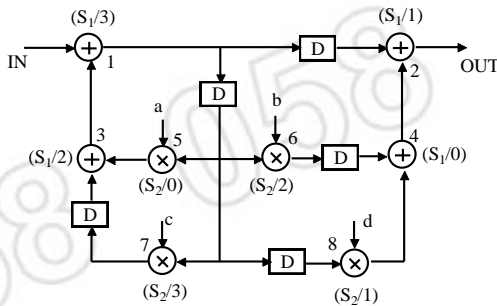
9. a) Construct a 2x2 convolution algorithm using Cook - Toom algorithm with $\beta = 0, \pm 1$. **10**

b) Explain steps in modified Cook-Toom algorithm. **4**

<div align="center">OR</div>

10. Construct 2x3 linear convolution algorithm using winograd algorithm with $m(p) = p(p-1)(p^2-1)$. **14**

11. a) Construct a 3x3 fast convolution algorithm by Inspection. **9**

b) Give Iterated convolution Algorithm. **4**

<div align="center">OR</div>

12. Construct a 4x4 cyclic convolution algorithm using CRT with $m(p) = p^4 - 1 = (p-1)(p+1)(p^2+1)$. **13**

<div align="center">**********</div>