B.E.(Electronics / Electronics & Telecommunication / Electronics Communication Engineering)
Semester Seventh (C.B.S.)

Advanced Digital System Design

P. Pages : 2 **KNT/KW/16/7446/7454**

Time : Three Hours * 0 8 2 0 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Discuss various levels of abstraction in VHDL. **6**

b) Explain the different design units used in VHDL with their syntax in brief. **7**

OR

2. a) Explain in brief history of VHDL and give its advantages. **7**

b) Write VHDL code of 2 input XOR gate using if statement. **6**

3. a) Explain in brief VHDL Data objects with suitable example. **7**

b) What are the scalar data type? Explain with examples. **7**

OR

4. a) Explain the difference between selected signal assignment and conditional signal assignment statements with example of 4 to 1 MUX. **7**

b) Design and write VHDL code for one bit full adder using Dataflow style. **7**

5. a) What is meant by subprogram? What are the types of subprogram. Explain in details. **7**

b) Write test bench for 1:8 demultiplexer. **6**

OR

6. a) Design a 16:1 MUX using 4:1 MUX using Generate statement. **7**

b) Write a VHDL code for 3:8 decoder using case statement. **6**

7. What is the basic difference between Moore and Mealy circuit? Design a sequence detector to detect the sequence of '1010' using Mealy machine. Use JK Flip-Flop. Also write the VHDL code for it. **14**

OR

8. Design a asynchronous circuit with two inputs x_1 and x_0 and single output z. So long as $x_0 = 0$, the output z is to be z = 0 and is not respond to change in x_1. The first change in x_1 which occure while $x_0 = 1$ is to cause z to become z = 1. Once z as gone to z = 1, z should again be unresponsive to x_1 and z should return to z = 0, only when x_0 return to $x_0 = 0$. Assume that x_1 & x_0 do not change at the same time. **14**

9. a) Define synthesis in VHDL? What are the steps of synthesis. **6**

b) Write short note on pipelining in VHDL. **7**

OR

10. Write short notes on **any two.** **13**

i) Partitioning for synthesis.

ii) Power Analysis in FPGA based system.

iii) Resource sharing.

11. a) Implement a combinational circuit defined by the function **7**

$$F_1(A, B, C) = \Sigma(3, 5, 6, 7)$$

$$F_2(A, B, C) = \Sigma(0, 2, 4, 7)$$

by using 3x4x2 PLA.

b) Write a short note on XC4000 series FPGA. **6**

OR

12. a) Write VHDL code for 4-bit Barrel shifter that shift the data left by 1-bit. **7**

b) Write VHDL code for 3-bit multiplier using structural style. **6**

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