P. Pages : 2

KNT/KW/16/7290

Time : Three Hours

‖‖‖‖‖‖‖‖‖‖‖‖
* 0 1 5 8 *

Max. Marks : 80

_____

Note :   1.   All questions carry marks as indicated.
2.   Solve Question 1 OR Questions No. 2.
3.   Solve Question 3 OR Questions No. 4.
4.   Solve Question 5 OR Questions No. 6.
5.   Solve Question 7 OR Questions No. 8.
6.   Solve Question 9 OR Questions No. 10.
7.   Solve Question 11 OR Questions No. 12.
8.   Due credit will be given to neatness and adequate dimensions.
9.   Assume suitable data whenever necessary.
10.   Illustrate your answers whenever necessary with the help of neat sketches.

1.   a)   Explain memory segmentation of 8086 along with its advantages.   **7**

b)   Write 8086 ALP to move string of <u>data</u> <u>words</u> from offset 1234H to offset 5678H, the length of string is <u>10</u>.   **7**

OR

2.   a)   Explain physical address formation in 8086 with one example.   **7**

b)   Interface 16 KB RAM and 16 KB ROM to 8086 (minimum mode). Assume suitable starting addresses.   **7**

3.   a)   Interface 8 ON/Off switches with 8086 microprocessor.   **7**

b)   Draw and explain block diagram of 8253 PIT.   **6**

OR

4.   a)   Interface DAC with 8086 in minimum mode and write a program to generate a triangular waveform at the output of DAC.   **7**

b)   Draw and explain the interfacing of 4x4 matrix keyboard with 8086.   **6**

5.   a)   Draw and explain block diagram of 8255 PPI.   **7**

b)   Explain internal diagram of 8259 PIC.   **6**

OR

6.   a)   Explain all ICW's and OCW's of 8259.   **6**

b)   Draw and Explain internal block diagram of 8251 USART.   **7**

7.	a)	Draw and explain 8087 NDP architecture.	**7**
	b)	Explain 8289 bus arbiter.	**7**

OR

8.	a)	Explain keyboard and display modes of 8279 PKDC.	**7**
	b)	Interface 8237 PDMAC with 8086.	**7**
9.	a)	Explain the memory organization of 8051.	**7**
	b)	Explain the PSW of 8051.	**6**

OR

10.	a)	Explain the concept of paging.	**7**
	b)	Explain real and protected mode.	**6**
11.	a)	Give differences between CISC and RISC.	**7**
	b)	What is Task State Segment (TSS)? How it is addressed?	**6**

OR

12.	a)	Explain the Pentium architecture.	**7**
	b)	Explain IDT descriptors.	**6**

****