B.E. Eighth Semester (Electronics & Communication / Electronics & Telecommunication Engineering) (C.B.S.)

Elective - III : CMOS VLSI Design

P. Pages : 2 **KNT/KW/16/7570**

Time : Three Hours * 0 2 7 9 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.
11. Use of non programmable calculator is permitted.

1. a) Explain the operation of nMOS enhancement transistor. Hence explain the pinch off phenomenon. **7**

b) Derive MOS device equations (DC) for drain to source current (Ids) Vs Drain to source voltage (Vds) in three regions of operation. **6**

OR

2. a) Calculate the native threshold voltage for an n-transistor at 300ºK with $N_A = 1.8 \times 10^{16} cm^{-3}$, SiO_2 gate oxide with thickness $200\,\overset{o}{A}$ (Assume, $\phi_{ms} = -0.9V$, $\phi_{fc} = 0$) **7**

b) Explain the small signal equivalent model for a MOS transistor. **6**

3. a) Explain the five regions of operation of CMOS inverter D.C transfer characteristic. Hence write the equations for V_{out} in the different regions. **9**

b) Explain the operation of BICMOS inverter. **5**

OR

4. a) Calculate the Noise Margin for a CMOS Inverter operating at 3.3V with $V_{th} = 0.7V$, $V_{tp} = -0.7V$, where $\beta_h = \beta_p$. What changes can be made in VTC of CMOS inverter to improve Noise Margin. **8**

b) Design following functions using transmission gate **6**
i) 2 : 1 MUX
ii) EX – OR gate

5. a) Design CMOS compound gates for the following functions : **6**

i) $F = \left(\overline{(A \cdot B) + (C \cdot D)}\right)$

ii) $F = \left(\overline{((A \cdot B) + C) \cdot D}\right)$

iii) $F = \left(\overline{(A \cdot B \cdot C) + D}\right)$

b) Design a CMOS positive edge triggered D flip flop. **7**

OR

6. a) Design a 4 input multiplexer using CMOS switches. **6**

b) Explain SRAM & DRAM. **7**

7. a) Explain capacitance estimation of MOS device indicating accumulation depletion, inversion and explain its variation as a function of Vgs. **7**

b) Describe static power dissipation, dynamic dissipation, short circuit dissipation and hence total power dissipation. **7**

OR

8. a) For switching characteristics for CMOS inverter define : **6**

i) RISE time

ii) FALL time

iii) Delay time

b) Suggest schemes to reduce rise and fall time of an inverter. **4**

c) Explain Charge Sharing. **4**

9. a) Draw the stick layout for the function $Z = \overline{A + BC + DE}$ using CMOS logic. Also draw Euler's graph and find the Euler's path. **7**

b) What is Latch up? How it can be prevented? **6**

OR

10. a) Explain the terms : **4**

i) Fan in,

ii) Fan out for CMOS

b) Explain clocking strategies in CMOS. **9**

11. a) State and Explain types of Faults. **7**

b) Explain need for Design for testability. **6**

OR

12. a) Explain Built In Self Test (BIST) **7**

b) Explain Boundary Scan. **6**

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