B.E.(Electronics Engineering / Electronics Telecommunication / Electronics Communication Engineering) Semester Fifth (C.B.S.)

Analog Circuits and Design

P. Pages : 3 **KNT/KW/16/7325/7330**

Time : Three Hours * 0 6 4 5 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.
11. Use of non programmable calculator is permitted.

1. a) Draw and explain block diagram of an Op – Amp. **6**

b) Design dual input, balanced output differential amplifier for the following specifications: **7**
R_C = 2.2 K Ω, R_E = 4.7 K Ω, V_{CC} = 15 V, V_{EE} = -15 V and transistor having β = 100 and V_{BE} = 0.6 V.

i) Determine the ICQ and VCEQ

ii) Determine the voltage gain

iii) Determine input and output resistance

OR

2. a) Define the following terms: **6**

i) CMRR ii) Slew rate

iii) input offset current iv) Gain Bandwidth product

b) For an inverting amplifiers following data are given: **7**
$A = 2 \times 10^5$; R_i = 2M Ω, R_O = 75 Ω, R_1 = 470 Ω, R_F = 4.7 K Ω, UGB = 1 MHz,
Supply voltages = ±15 V; maximum O/P
Voltage swing = ±13 V;

Calculate:

i) Closed loop gain, ii) input resistance with feedback iii) output resistance with feedback and iv) Bandwidth with feedback.

3. a) Design an op amp circuit to implement the following specification or expression **7**

$V_0 = 3V_1 - 2V_2 + 2V_3 + 2V_4$

Assume $R_F = 100\ K\ \Omega$

b) Draw the circuit of instrumentation amplifier using three op amp and derive the expression for output voltage V_0. **7**

OR

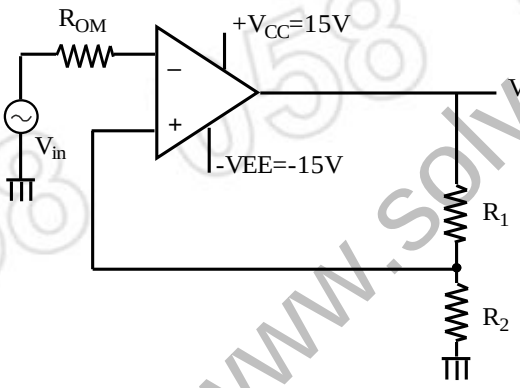
4. a) Design integrator circuit to implement following equations: **6**

$$V_0 = \frac{-1}{3}\int V_1\,dt\ \frac{-1}{2}\int V_2\,dt - \int V_3\,dt$$

Where V_1, V_2 and V_3 are input voltages & V_0 is the O/P voltages

b) Draw the circuit of practical temperature compensated logarithmic amplifier and derive an expression for output voltage. **8**

5. a) For a Schmitt trigger circuit using op amp. Shown in fig (5) a. find out the value of VLT & Vut & VH. Assume R_1= 82 K Ω; R_2 = 2K Ω. **7**



Assume Vsat = ±12V.

b) Draw & explain precision full wave rectifier. **6**

OR

6. a) Design as table multivibrator using IC 555 to generate square wave output with 50% duty cycle at 5 KHz. Assuming capacitor = 0.01 μF **7**

b) Draw and explain R – 2R ladder type D to A Converter. **6**

7. Design SVR to give 5 V output at maximum load current of 200mA. Assume that unregulated input is 12 V ± 10% V with source resistance 1 Ω. Determine Sv & Ro. Assume transistor having $h_{fe_1} = 60$ and $h_{fe_2} = 100$. **14**

OR

8. Design a stepdown SMPS to give 5V. $I_O = I_L = 8$ Amp. unregulated input is 20 V, switching frequency is 25 KHz. Assume reference voltage is 2V. Vsat = 1.2 V. tsw = 1.1 µsec. & V_{DON} = 1V. The output ripple should be limited to less than 80mV(P-P). Also calculate the efficiency of SMPS. **14**

9. a) Design Rc phase shift oscillator for the following specifications: **7**
V_0 8 V peak to peak, frequency of oscillations = 10 KHz, Also determine frequency shift if phase shift of 1° is introduced in the loop.

b) Derive the frequency of oscillation for wein bridge oscillator. **6**

OR

10. a) Derive an expression for figure of merit for Hartley oscillator. **8**

b) Write a technical short notes on design of diode function generator. **5**

11. a) Design Butterworth filter such that relative attenuation is less than 1dB for frequencies below 500 Hz and greater than 17 dB for frequencies above 1 KHz. **7**

b) Design 4^{th} order high pass filter with cut off frequency of 8 KHz. **6**
(Assume C = 0.1 µF)

OR

12. a) Design a bandpass filter using IGMF techniques to give a band pass gain 5 centre frequency 8 KHz and bandwidth 1 KHz. Calculate the value of R_2. **7**

b) Write short note on **any one.** **6**

i) Design of Relay driver circuit.

ii) Design of First order LPF.

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