Third Semester B. E. (CSE) (CBS) Examination

COMPUTER ARCHITECTURE AND ORGANISATION

Time : Three Hours] [Max. Marks : 80

N. B. : (1) All questions carry marks as indicated.

(2) Solve **Six** questions as follows :
Que. No. 1 OR Que. No. 2
Que. No. 3 OR Que. No. 4
Que. No. 5 OR Que. No. 6
Que. No. 7 OR Que. No. 8
Que. No. 9 OR Que. No. 10
Que. No. 11 OR Que. No. 12

(3) Due credit will be given to neatness and adequate dimensions.

(4) Illustrate your answers wherever necessary with the help of figures / drawings.

1. (a) Consider the following possibilities for saving the return address of an subroutine.

(i) In a process register.

(ii) In a memory location associated with the call, so that different location is used when subroutine is called from different places.

(iii) On a stack.

Which of there possibilities supports supportive nesting and which supports subroutine recursion and why ? 7

(b) Register R5 is used in a program to point the top of stack containing 32-bit number. Write a sequence of instruction using Index Auto increment and Auto decrement addressing modes to program each of following tasks :—

(i) POP two items off the stack, add them and push result onto stack.

(ii) Copy fifth element from top into register R3.

(iii) Remove top ten items from the stack.

For each case, assume stack contains ten or more elements. 7

OR

2. (a) Explain various bus structures of computer. 7

(b) Explain various addressing modes with examples which are used in instruction set-design. 7

3. (a) Write and explain carry look ahead addition with circuit diagram. 6

(b) Multiply the following with the help of Booths algorithm (–13) x (11) 7

OR

4. (a) Represent :—

(i) $(-450.725)_{10}$

(ii) –0.000125

(iii) 3.295×10^2

in double precision IEEE format. 6

(b) Explain circuit arrangement for binary division. 7

5. (a) Short note on (Any **Two**) :—

(i) Memory interleving.

(ii) Associative memory.

(iii) Page table and page replacement. 6

(b) Draw the block diagram to implement 8M x 32 memory using 512 k x 8 memory chips. 7

OR

6. (a) A block set associative cache consist of a total of 64 blocks sets. The main memory contains 4096 blocks each consisting of 128 words.

(i) How many bits are there in a main memory address.

(ii) How many bits are there in each of the TAG, SET and WORD fields. 7

(b) Explain virtual memory system and concept of locality of reference with their types. 6

7. (a) What is Bus arbitration ? Explain their type in detail with diagram. 7

(b) Explain Magnetic disk, its operations and working of CD-ROM. 6

OR

8. (a) Explain interrupts with their types. 7

(b) Write a program that display the contents of 10 bytes of the main memory in hexadecimal format in a video display. Start at location LOC in the memory and use two hex character per byte. 6

9. (a) What mechanism a pipelined machine must provide for dealing with branch instruction ? Explain with example. 7

(b) Give the features of RISC and CISC architectures. 6

OR

10. (a) A program loop ends with a conditional branch to the beginning of the loop. How would you implement this loop on a pipelined computer that are a delay branching with one delay slot ? Under what condition would you be able to put useful instruction in the delay slot ? 7

(b) Explain data dependency in detail with example. 6

11. (a) What is the need of parallel processing ? Explain the classification of parallel architecture. 7

(b) Explain multicase architecture with suitable diagram. 7

OR

12. Short note on (Any **Two**) :—

(i) Array processor.

(ii) Vector processor.

(iii) Array processor. 14