10. Write short notes on any **TWO** :

(a) Pipelining in VHDL

(b) Resource Sharing

(c) Power Analysis in FPGA based system.

(d) Timing Analysis of Logic Circuits. 13

11. (a) Write a short note on XC4000 series FPGA. 7

(b) Implement the following function using PLA :

F1(A, B, C, D) = $\dot{\Sigma}$ m (0, 1, 4, 5, 9, 10, 11)

F2 (A, B, C, D) = $\dot{\Sigma}$ m (0, 1, 2, 3, 4, 5, 8, 9, 10, 11)

F3(A, B, C, D) = $\dot{\Sigma}$ m (4, 5, 6, 7, 8, 9) 7

**OR**

12. (a) Write VHDL Code for 4-bit shift left barrel shifter. 7

(b) Write a VHDL Code for 4-bit ALU. 7





**Faculty of Engineering & Technology**
**Seventh Semester B.E. (Electronics Engg.)ET/EC**
**(C.B.S.) Examination**
**ADVANCED DIGITAL SYSTEM DESIGN**

Time—Three Hours] [Maximum Marks—80

**INSTRUCTIONS TO CANDIDATES**

(1) All questions carry marks as indicated.

(2) Solve Question No. **1 OR** Questions No. **2**.

(3) Solve Question No. **3 OR** Questions No. **4**.

(4) Solve Question No. **5 OR** Questions No. **6**.

(5) Solve Question No. **7 OR** Questions No. **8**.

(6) Solve Question No. **9 OR** Questions No. **10**.

(7) Solve Question No. **11 OR** Questions No. **12**.

(8) Due credit will be given to neatness and adequate dimensions.

(9) Illustrate your answers wherever necessary with the help of neat sketches.

1. (a) What are the advantages of VHDL over other conventional programming languages ? 5

(b) What do you mean by Modelling Styles ? What are different modelling styles used in VHDL ? Explain. 8

**OR**

2. (a) Explain in detail, with suitable flow chart about the development of digital system with VHDL. 7

(b) Write a VHDL code for gate level 4 : 1 multiplexer. 6

3. (a) Explain various data types supported by VHDL. 7

(b) Write short notes on any **two** :

(i) Architecture

(ii) Entity

(iii) Package. 6

**OR**

4. (a) Write a VHDL Code for 3 : 8 decoder using CASE statement. 5

(b) What are different data objects used in VHDL ? Explain. 5

(c) Write a VHDL code for 'Half Adder' using 'IF-Else' statement. 3



5. (a) What are the different types of subprograms used in VHDL ? Explain them in detail. 7

(b) Write a VHDL code for 4-bit ripple carry adder using 'GENERATE' statement. 7

**OR**

6. (a) Write a test bench for 'Full adder'. 6

(b) Write the structural description of 16 : 1 MUX using 4 : 1 MUX using VHDL. 8

7. (a) What is the basic difference between Moore and Mealy Circuit ? 3

(b) Design a sequence detector to detect the sequence '111' using Moore machine. Use flip flop. Also write the VHDL code for it. 10

**OR**

8. Design a fundamental mode sequential circuit with two inputs $x_1$ and $x_2$ and one output Z. The output Z =1 if both inputs $x_1$ and $x_2$ are equal to 1, but only if input $x_1$ becomes one before input $x_2$. 13

9. (a) What is Synthesis in VHDL ? Explain synthesis design flow in VHDL. 7

(b) Write a short note on "Partitioning for synthesis". 6

**OR**