8. (a) Explain all directory based protocols used for cache coherence. 9

(b) Explain in brief the following terms for interconnection networks

(i) Node degree

(ii) Bisection width

(iii) Network Latency

(iv) Bandwidth

(v) Diameter of a Network. 5

9. (a) Explain various vector instructions that can be executed on a vector processor. 8

(b) What are dataflow architectures ? 5

OR

10. (a) What are the principles followed for vector processing ? 6

(b) Explain Scalable multithreaded organization. 7

11. (a) How compilation technique will help parallel programming ? 7

(b) Explain the role of dependence analysis in parallel programming. 6

OR

12. (a) What are different parallel language constructs available ? 7

(b) Write a short note on code optimization and scheduling. 6

NTK/KW/15/7576

Faculty of Engineering & Technology
Seventh Semester B.E. (C.S.E.) (C.B.S.) Examination
ELECTIVE–I : ADVANCED COMPUTER ARCHITECTURE

Time—Three Hours] [Maximum Marks—80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.

(2) Solve Question No. **1 OR** Questions No. **2**.

(3) Solve Question No. **3 OR** Questions No. **4**.

(4) Solve Question No. **5 OR** Questions No. **6**.

(5) Solve Question No. **7 OR** Questions No. **8**.

(6) Solve Question No. **9 OR** Questions No. **10**.

(7) Solve Question No. **11 OR** Questions No. **12**.

(8) Illustrate your answers wherever necessary with the help of neat sketches.

(9) Use of non-programmable calculator is permitted.

1. (a) With neat diagrams explain the architectures of processors proposed by Flynn. 8

(b) How shared memory multiprocessors are categorized ? 5

OR

2. (a) Explain different types of dependencies and draw dependence graph for the following set of segments :

S 1 : C = D * E
S 2 : M = G + C
S 3 : A = B + C
S 4 : C = L + M
S 5 : F = G + E

What are different grain sizes ? 9

(b) What are the advantages of grain packing ? 4

3. (a) Explain Amdahl's law for operation speed up in a processor. 5

(b) The main memory of a computer is organized as 64 blocks, with a block size of 8 words. When cache has 8 blocks frames.

Show the mapping from main memory to cache memory according to the following techniques with calculation of no. of bits for address field.

(i) Direct mapping
(ii) 2 way set associative
(iii) Fully associative. 9

OR

4. (a) Explain typical architecture of a vector processor with neat sketch. 5

(b) Explain following properties of cache memory.

(i) Inclusion
(ii) Coherence
(iii) Locality of reference. 9

5. (a) Explain synchronous and asynchronous linear pipeline processor. 3

(b) Consider the following reservation table for a 3 stage pipelined processor and answer the following :

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X	X		

(i) What are forbidden latencies ?
(ii) What is collision vector ?
(iii) Draw state transition diagram.
(iv) List all simple cycles and greedy cycles.
(v) What is MAL ? 10

OR

6. (a) Explain execution of following instructions on a 7 stage pipeline. How many cycles will be required for execution ?

X = Y + Z and A = B * C. 8

(b) Write a note on super scalar and super pipeline design. 5

7. (a) What do you mean by static and dynamic interconnection networks. List the various ways to design the inter-connection Networks. 8

(b) List the protocols used for cache coherence and explain snoopy bus protocol. 6

OR