B.E. (Electronics & Telecommunication / Electronics & Communication Engineering)
Seventh Semester (C.B.S.)

Elective - I : VLSI Signal Processing

P. Pages : 2 **TKN/KS/16/7545**

Time : Three Hours * 1 0 3 6 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Assume suitable data whenever necessary.
9. Use of non programmable calculator is permitted.

1. a) Explain how pipelining can be used for reducing power consumption. **4**

b) Consider the 4 tap filter shown in figure (a). Draw its two way parallel version. What can power saving be achieved if we maintain the same sampling rate? **9**

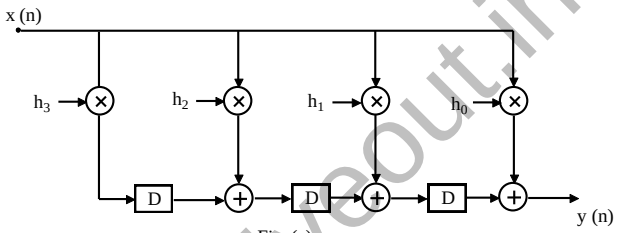


Fig. (a)

OR

2. a) Explain Parallel processing for Low Power. **6**

b) Design a parallel system with **7**
L (level of parallel processing) = 3
n (iteration factor) = 3 k
where k = no. of clock cycle.

3. a) Explain properties of Retiming. **4**

b) Consider the data flow graph, construct the matrix W(U, V) and D (U, V) by manual inspection construct the set of unequilities for clock cycle of 2. Solve the unequilities by creating a constraint graph and using Bellman – Ford algorithm find retimed graph. **10**

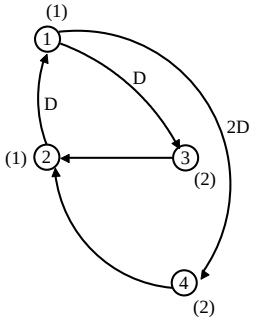
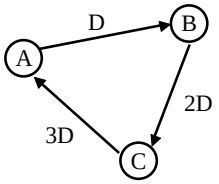


Fig. (b)

OR

4. Explain in detail : **14**
a) Retiming for clock period minimization. b) Retiming for Register minimization.

5. a) Unfold the DFG shown in figure below using unfolding factor 4. **9**



b) Explain in short unfolding Transformation. **4**

OR

6. a) Explain how unfolding can be used to design word level parallel processing. **8**

b) Give the properties of unfolding. **5**

7. a) Explain register minimization in folded architectures. **5**

b) Consider a DSP program that perform the transpose operation of 3 x 3 matrix, find minimum number of registers required to implement the DSP program & give its folded architectures. **8**

$$\text{The Matrix} = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix}$$

OR

8. a) Explain the procedure for folding of multirate system. **5**

b) Design folded biquad filter by systematic folding technique for the figure shown below. **8**

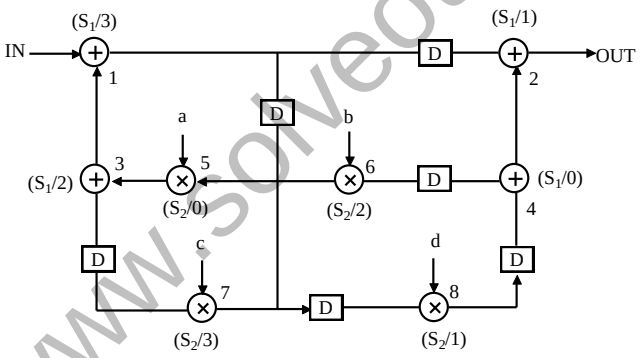


Fig. (c)

9. a) Construct a 2 x 2 convolution algorithm using Cook-Toom algorithm with $\beta = 0, \pm 1$ **10**

b) What is the significance of Winograd algorithm. **4**

OR

10. a) Construct 2 x 3 linear convolution algorithm using Winograd algorithm with **14**

$$m(P) = P(p-1)\,(p^2-1)$$

11. a) Construct a 4 x 4 cyclic convolution algorithm using CRT with **13**

$$m(p) = P^4 - 1 = (p-1)\,(p+1)\,(p^2+1)$$

OR

12. a) Construct a 3 x 3 fast convolution algorithm by inspection. **9**

b) Give Iterated convolution Algorithm. **4**

****