B.E. (Computer Science & Engineering (New)) Third Semester (C.B.S.)

Digital Circuits & Fundamentals of Microprocessors Paper - III

P. Pages : 2 **TKN/KS/16/7327**

Time : Three Hours Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Simplify the Boolean equation using Boolean algebra **6**

$F(A,B,C) = (A+B)\left[\overline{\bar{A}\,(\bar{B}+\bar{C})}\right] + \bar{A}\,\bar{B} + \bar{A}\bar{C}$.

b) Simplify the following expression using k-map and realize the minimum expression using logic gates $F(A, B, C, D) = \Sigma m\ (0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ **7**

OR

2. a) Realize all logic gates using NAND gates. **7**

b) State and prove De Morgan's theorems. **6**

3. a) Design a code converter which will convert 4 bit binary number applied at the input into equivalent gray code. **7**

b) Implement the following function using 8:1 multiplexer. **7**

$F(A, B, C, D) = \Sigma m\ (0, 1, 2, 3, 11, 12, 14, 15)$

OR

4. a) Design a 2 bit digital comparator circuit using gates. States its applications. **7**

b) How will you implement full subtractor using two half subtractor and one OR gate. Explain? **7**

5. a) Draw and explain the working of J K flip flop. What is race around condition? Explain. **7**

b) Convert :

i) T flip flop to S – R flip flop. **3**

ii) S R flip flop to J K flip flop. **3**

OR

6.	a)	Write notes on:	
		i) Excitation table for flip flop.	**3**
		ii) Use of preset and clear terminals of flip flop.	**3**
	b)	Draw and explain how a latch can be used as 1 bit memory cell.	**4**
	c)	Describe the difference between edge triggered and level triggered flip flop.	**3**
7.	a)	Draw and explain 4 bit serial input and parallel output (SIPO) shift register.	**7**
	b)	Explain the working of Twisted Ring counter with suitable block diagram.	**6**

OR

8.	a)	Draw and explain 4 bit ripple counter with waveforms.	**6**
	b)	Design a synchronous counter for the following sequence $4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4$ Avoid lockout condition. Use J K flip flop for design.	**7**
9.	a)	Explain the classification of memories with their characteristics.	**5**
	b)	Draw and explain the architecture of 8085 microprocessor.	**8**

OR

10.	a)	Write a short note on programmable logic devices.	**6**
	b)	Give the format of Flag register in 8085. Explain each flag.	**7**
11.	a)	Draw and explain interrupt structure of 8085 microprocessor.	**6**
	b)	Write a program to find larger number out of two given number. The numbers are available in D and C. Store the result in "L" register.	**8**

OR

12.	a)	Draw the timing diagram for the CALL 3000H instruction.	**7**
	b)	Write a program to add two 16 bit data present in memory from location 2010 H and place the result starting at 2014 H.	**7**

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