B.E. (Computer Science Engineering (New)) Third Semester (C.B.S.)

Computer Architecture & Organization Paper - V

P. Pages : 2 **TKN/KS/16/7329**

Time : Three Hours * 1 0 8 7 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Draw and explain the single bus structure and discuss it's advantages and disadvantages. **7**

b) Draw and explain the block diagram of a microprogrammed control unit. **7**

OR

2. a) Explain, how nested subroutine call is implemented using processor stack? **7**

b) State the advantages of having auto increment and auto decrement addressing modes in assembly language instruction set. **4**

c) State the attributes of vertical and horizontal instruction formats. **3**

3. a) Give Booth's algorithm for multiplication of two binary numbers. Also draw the necessary circuit arrangement. **7**

b) Design a carry look ahead adder. **6**

OR

4. a) Perform the operation $08 \div 03$ using restoring integer division algorithm. **7**

b) Explain why non-restoring integer division method is better than restoring integer division method. **3**

c) Give double precision IEEE floating point format. **3**

5. a) Write a short note on multiple module memory system. **7**

b) Find the page hit and page fault ratio for the given page address stream using (i) Least recently used (ii) Optimal (iii) First in first out page replacement algorithm. Assume three page buffers. **6**
page address stream : 7,8,7,6,10,7,9,10,8,7,10,7.

OR

6.	a)	Consider a cache consisting of 128 blocks of 08 words reach and main memory of 32 K words. Explain the various mapping functions with reference to the above stated cache.	**7**
	b)	Draw and explain the internal structure of a cache.	**6**
7.	a)	Write a short note on direct memory access of data transfer.	**7**
	b)	Write a short note on Daisy chain scheme of resolving interrupt priority.	**6**

OR

8.	a)	Explain the working principal of CD-ROM and organisation of data on CD-ROM.	**7**
	b)	Explain in detail the sequence of action taken by the microprocessor when it is interrupted.	**6**
9.	a)	State and explain the various hazards in instruction pipelining with supporting example of each.	**7**
	b)	Draw a typical hardware for a four stage instruction pipeline and explain it.	**7**

OR

10.	a)	Explain instruction queue and prefetching with the help of necessary hard ware organization.	**7**
	b)	Discuss with supporting example, the hazards caused by conditional branch instruction in instruction pipelining.	**7**
11.	a)	Draw and explain the uniform and non-uniform memory access multiprocessor system.	**7**
	b)	Draw and explain cross bar inter connection network.	**6**

OR

12.	a)	Write a short note on array processors.	**7**
	b)	Draw and explain single bus interconnection network.	**6**

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