B.E.(Information Technology) Fourth Semester (C.B.S.) Computer Architecture & Organization Paper – IV

P. Pages: 2 Time: Three Hours			TKN/KS/16/7 Max. Mark	
	Notes	s: 1. 2. 3. 4. 5. 6. 7.	All questions carry marks as indicted. Solve question 1 or questions no. 2. Solve question 3 or questions no. 4. Solve question 5 or questions no. 6. Solve question 7 or questions no. 8. Solve question 9 or questions no. 10. Solve question 11 or questions no. 12.	
1.	a)	Explain	n functional units of a basic computer system.	6
	b)	Differe	entiate between the big endian assignment and little - endian assignment.	4
	c)	Explain	n the difference between multiprocessor and multicomputers.	4
			OR	
2.	a)	Explain	n straight line sequencing in detail. What is the function of MAR, MDR, ALU?	7
	b)		n 3-address, 2-address, 1- address and zero address instruction formats. Why there ed of small length instructions.	7
3.	a)	Explain	n the role of stack in subroutine call implementation with example.	6
	b)	Explain	n execution of complete instruction using three bus architecture.	7
			OR	
4.	a)	Enlist a	and explain with example the different addressing modes of 68000 processor.	8
	b)	Explain	n single bus organization of a data path of a processor with block diagram.	5
5.	a)	Explain	n the function of microprogram control unit.	6
	b)	Explain	n the difference between Hardwired and microprogrammed control unit.	4
	c)	List ou	t the application of microprogramming.	3
			OR	
6.	a)	•	ontrol signals are needed in a CPU to execute an instruction? write a control signal tion for ADD R0, R1 where result is stored in R0.	7
	b)		s horizontal and vertical μ-instruction format? Explain grouping of control signals suitable example.	6

a)	Why 2's compliment number representation is used over other methods of negative number representation?	3			
b)	Explain the design of fast address.	5			
c)	Write short note on how arithmetic operations are performed in floating point numbers.	5			
	OR				
a)	Multiply the following pair of signed 2's complement number using Booths multiplication and bit pair recording technique. $A = 010111, B = 110110$ Where A is multiplicand & B is multiplier				
b)	Solve 1010 DIV 0101 using non restoring division algorithm.				
a)	Explain with the help of neat sketch the structure of dynamic RAM cell. Also discuss its advantages over static RAM cell.				
b)	Explain virtual memory. Also explain how virtual address is translated into physical address.	7			
	OR				
a)	Explain the various mapping techniques used in cache memory	8			
b)	Differentiate between i) RAM and ROM. ii) RISC and CISC architecture.	6			
a)	Define interrupts. Explain in detail different types of interrupts.	4			
b)	Explain the block diagram of two channel DMA controller.				
c)	Explain the difference between memory mapped I/O and I/O mapped I/O.	4			
	OR				
a)	What are tightly and loosely coupled systems? Explain.				
b)	Explain the following. i) Array processors. ii) Online storage. iii) Pipelining. iv) Memory Interleaving.	8			
	b) c) a) b) a) b) c) a) c) a) a) b) c)	number representation? b) Explain the design of fast address. c) Write short note on how arithmetic operations are performed in floating point numbers. OR a) Multiply the following pair of signed 2's complement number using Booths multiplication and bit pair recording technique. A = 010111, B = 110110 Where A is multiplicand & B is multiplier b) Solve 1010 DIV 0101 using non restoring division algorithm. a) Explain with the help of neat sketch the structure of dynamic RAM cell. Also discuss its advantages over static RAM cell. b) Explain virtual memory. Also explain how virtual address is translated into physical address. OR a) Explain the various mapping techniques used in cache memory b) Differentiate between i) RAM and ROM. ii) RISC and CISC architecture. a) Define interrupts. Explain in detail different types of interrupts. b) Explain the block diagram of two channel DMA controller. c) Explain the difference between memory mapped I/O and I/O mapped I/O. OR a) What are tightly and loosely coupled systems? Explain. b) Explain the following. i) Array processors. ii) Online storage.			
