Fourth Semester B. E. (Information Technology and Computer Engg.). Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Time: Three Hours] [N	fes. Marks: 80
N. B.: (1) All questions carry marks a 12) Assume suitable data whereve (3) Bustrate your answers whereve the help of near skerches	
 (a) What is straight line sequencing? 	Explain 4
(b) Explain in brief the functional unit system.	ts of computer
(c) Explain single bus structure. Flow is achieved between processor and s output devices.	synchronization low input and 5
OR	
2. (a) Explain with one address, two address instruction, the following ex	ress, and three
Z=(A+B-C)*(C-D+E)/(A*B (b) Explain different addressing mode with	-C) -
madessing mode wi	
3. (a) What are the limitations of short machine?	word length
(b) Explain condition code flag of 6800	
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instruction ADD (R ₃), R ₁ 5
OR
4. (a) Explain different instruction set available in computer systems with suitable example. 5
(b) Write in short about :—
(i) Subroutine linkages
(ii) Three bus architecture. 8
5. (a) Explain microprogram control unit for microin- struction with diagram.
(b) Write microprogram for instructions ADD (R ₄), R ₅ . using single bus organization.
(c) What is Bit slicing? Explain in brief. 4
OR
6. (a) Compare microprogram control unit with Hardwired control unit.
(b) What are various microinstruction format supported by microprogrammed control unit?
(c) Explain how emulation facilitates transmission into new system with a minimum of disruption. 4
7. (a) Explain the design of fast adder. 7
(b) Give the IEEE 754 floating point format for single and double precision for the following
(i) -1.5 (ii) -5 7
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8.	(a)	Perform the following multiplication using Booth's algorithm for signed operand multiplication 11x-6.
	(b)	Discuss arithmetic and branching conditions of
	(c)	number representation. What are guard bits? Also explain rounding off technique and mention four policies of it. 4
9.		Explain in detail about various mapping techniques 9 used in cache memory.
	(b)	Explain in brief about utility of memory interleaving and multimodeling.
		OR
10.		Explain how address translation is done in virtual memory.
	(b)	Write difference between static and dynamic RAM.
*.	(c)	Design and draw 128 m x 8 memory using 2 m x 4 memory chip.
11.	(a)	· How data transfer takes place using DMA technique.
	(b)	Explain various interrupt handling technique.
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OR

- 12. (a) List all the characteristic feature of RISC and CISC processor.
 - (b) Write a short note on (any three) :-
 - (i) Pipelining.
 - (ii) Online storages.
 - (iii) Array processor.
 - (iv) . File services.
 - (v) DATA Dependancy.

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